SEMINAR NOTICE:

Performance optimization for embedded signal processing platform with multiple coprocessors system and parallel computing

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Abstract:
Nowadays, embedded systems are widely used in the academic and industrial applications. With the powerful processors technology, embedded systems are able to deliver high throughput with small hardware platforms. In this talk, we are going to discuss that multiple processors are involved concurrently due to the complex design. For some signal processing applications, the performance and power consumptions are both critical requirements. It is important to optimize the hardware architecture of processors and enable parallel computing, to boost the performance with relative low power consumption. Some optimization techniques for different processors will be discussed in this talk as well.

Biosketch:
Dr. Qi CAO pursued his Ph.D. study in Nanyang Technological University from 2002 to 2005. Earlier, he graduated with Bachelor of Engineering degree from HuaZhong University of Science & Technology, China in 2000, where he obtained "Outstanding Graduate Award of the University." He had 2 years post-doc research experience at Institute for Infocomm Research, A*STAR, Singapore, and he also had 7 years industrial working experience. His interests focus on hardware architecture of embedded processors, reconfigurable computing for multiple processors system and high speed embedded systems involving FPGA, DSP, micro-processor and GPU.